

REMARKS

This paper is in response to the Office Action dated April 4, 2003. Claims 1-35 are currently pending. Reexamination and reconsideration are respectfully requested.

Claims 1-5, 7-9, 23 and 32 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,652,450 to Hirano in view of Takeda et al (JP 09321156). The rejection is respectfully traversed. Applicant notes that the Examiner cited specific portions of the Takeda reference, which is in Japanese. Applicant is not sure but assumes that the Examiner is referring to U.S. Patent No. 5,939,749 to Taketa et al. ("Taketa"), which appears to rely for priority on JP 8-258980, which is the application number for JP 09321156.

The Examiner on page 18 of the Office Action stated that "applicant cites no specific section of Hirano that states that Hirano has overcome the problem of excess charge extraction from the floating gates during erase mode. On the other hand, Takeda et al specifically discloses that a split gate may be directly substituted for a stacked gate such as the stacked gate used in Hirano, to prevent excess charge extraction from the floating gates during erase mode." citing Takeda at paragraphs 3-4. Taketa does state that "As one solution to avoid the excess erasure of the stacked gate memory cells, split gate memory cells have been developed." Taketa at col. 1, paragraph 4. However, Taketa also appears to disclose other ways to prevent the excess erasure. Takeda, prior to mentioning the use of a split gate memory cell, states that "To prevent this excess erasure, the erasing procedures of the individual memory cells should be controlled by a peripheral circuit of the memory device or by an external circuit connected to the memory device." Taketa at col. 1, paragraph 3 (lines 33-37). Applicant respectfully submits that Hirano uses such a structure including a "peripheral circuit of the memory device or by an external circuit connected to the memory device." For example, it appears that such peripheral circuits or external circuits are described throughout Hirano, including, for example, from column 9 through column 17. Fig. 10 of Hirano shows circuits including driver circuit 1, applied voltage decoder 2, control voltage decoder 3, substrate voltage control circuit 5, and negative voltage supply circuit 4. The various circuits operate in a manner dependent on the operational mode. The use of the various circuits in the erasure mode is described throughout the Hirano specification in columns 9-17.

As a result, one of ordinary skill, in reading Hirano and Taketa, would realize that Hirano solves any problem relating to "excess erasure" by the use of a "peripheral circuit of the memory device or by an external circuit connected to the memory device." (citing Taketa at col. 1, paragraph 3, lines 33-37) Thus, one of ordinary skill would have no motivation to modify Hirano to insert a split-gate structure from Takeda as suggested by the Examiner. Accordingly, the Examiner's basis for the rejection does not meet the legal standard for establishing obviousness and applicant respectfully submits that the rejection of claims 1-5, 7-9, 23 and 32 should be withdrawn.

In addition, applicant also respectfully submits that the Examiner's citations to Takeda do not clearly establish that "a split gate may be directly substituted for a stacked gate such as the stacked gate used in Hirano" as stated on pages 4 and 18 of the Office Action. Other structural and processing aspects, for example, the shape and position of the source and drain regions, the size of the split gate versus the stacked gate, the order of forming various layers in the structure, and other factors, may lead to a split gate structure as described in Takeda not being a direct substitution for the stacked gate structure of Hirano due to the effects of such a substitution on other features of the Hirano structure and processing scheme. Thus, applicant respectfully submits that the rejection of claims 1-5, 7-9, 23 and 32 should also be withdrawn for this reason.

Applicant notes that the Examiner stated on page 17 of the Office Action that "claim 32 is independent of claim 1 and present a completely different claim. Patentability of claim 1, in an of itself, is not reason to conclude claim 32 is patentable. Since applicant does not argue patentability of claim 32 it is concluded that applicant concedes that claim 32 is unpatentable." As noted by the Examiner, applicant had stated in the previous response that the rejection of claim 32 ". . . should be withdrawn for at least the same reason as claim 1." Applicant does not understand the Examiner's comments, because applicant was stating that a similar rationale used to overcome the rejection of claim 1 could also be used for claim 32. Applicant has not and does not concede that claim 32 is unpatentable.

Claim 31 was rejected under 35 U.S.C. 103(a) as unpatentable over Hirano in view of Takeda and U.S. Patent No. 6,242,773 to Thomas. The rejection is respectfully traversed. Thomas does not overcome the insufficiency of the Examiner's rationale to support the proposed combination of Hirano and Takeda as explained above in the discussion of the rejection of claims

1-5, 7-9, 23 and 32. Thus, for at least the same reasons as discussed above, the rejection of claim 31 should be withdrawn. Applicant notes that the Examiner stated on pages 17-18 of the Office Action that "applicant sets forth no arguments for patentability of claim 31. Since applicant does not argue patentability of claim 31 it is concluded that applicant concedes that claim 31 is unpatentable." As noted by the Examiner, applicant had stated in the previous response "that for reasons at least similar as claim 1, the rejection of claim 31 should be withdrawn." Applicant does not understand the Examiner's comments, because applicant was stating that a similar rationale used to overcome the rejection of claim 1 could also be used for claim 31. Applicant has not and does not concede that claim 31 is unpatentable.

Applicant also submits that one of ordinary skill would not combine Thomas with Hirano and Takeda as suggested by the Examiner. The Examiner stated on pages 5-6 of the Office Action that "it would have been obvious . . . to replace the single layer of Hirano's memory cell with the ONO layer such as taught by Thomas in order to allow the intermediate insulation layer and the floating gate to be simultaneously patterned and self-aligned on the control gate to thus provide better more efficient manufacture." As described in Thomas and shown in Thomas Figs. 1B-1E, it appears that the insulation layers (including at least layers 120 and 118) are formed to be self aligned with the side surfaces 122A and 122B of the floating gate layer 116. However, the Examiner proposed to form a split-gate structure in Hirano. A split gate structure such as shown in Takeda appears to have insulating layers that are not self-aligned with the side surfaces of the floating gate as shown in Thomas. Thus, the Examiner's rationale for the combination, including ". . . simultaneous patterned and self aligned. . ." is not consistent with forming the split gate structure. Accordingly, one of ordinary skill would have no motivation to make the combination with Thomas as suggested by the Examiner. Thus, applicant respectfully submits that the rejection of claim 31 should also be withdrawn for this reason.

Claims 10-11, 16-20, 25 and 28-30 were rejected under 35 U.S.C. 103(a) over Hirano in view of Takeda and U.S. Patent No. 5,654,577 to Nakamura et al. and U.S. Patent No. 5,650,344 to Ito et al. The rejection is respectfully traversed. The Examiner's addition of Nakamura and Ito do not overcome the insufficiency of the Examiner's rationale for the combination of Hirano and Takeda as discussed above. Thus, for at least similar reasons as explained above, the rejection of claims 10-11, 16-20, 25 and 28-30 should be withdrawn.

Claims 12-14 and 21 were rejected under 35 U.S.C. 103(a) over Hirano in view of Takeda and Nakamura and Ito and Thomas. The rejection is respectfully traversed. The Examiner's addition of Nakamura, Ito and Thomas do not overcome the insufficiency of the Examiner's rationale for the combination of Hirano and Takeda as explained above in the discussion of the rejection of claims 1-5, 7-9, 23 and 32. Thus, for at least similar reasons as explained above, the rejection of claims 12-14 and 21 should be withdrawn.

Applicant also respectfully submits that the Examiner's rationale for the proposed combination of Thomas with Hirano and Takeda would not be made by one of ordinary skill in the art as explained above in the discussion of claim 31. Thus, the rejection of claims 12-14 and 21 should also be withdrawn for this reason.

Claim 8 was rejected under 35 U.S.C. 103(a) over Hirano in view of Takeda and U.S. Patent No. 4,688,063 to Lu et al. ("Lu"). The rejection is respectfully traversed. The Examiner's addition of Lu does not overcome the insufficiency of the Examiner's rationale for the combination of Hirano and Takeda as explained above in the discussion of the rejection of claims 1-5, 7-9, 23 and 32. Thus, for at least similar reasons as explained above, the rejection of claim 8 should be withdrawn.

Applicant also does not understand the Examiner's comments on page 19 of the Office Action relating to claims 10-11, 16-20, 25 and 28, and to claims 12-14 and 21. As explained above for claims 31 and 32, applicant was stating that a similar rationale used to overcome the rejection of claim 1 could also be used for claims 10-11, 16-20, 25 and 28, and for claims 12-14 and 21. Applicant has not and does not concede that claims 10-14 16-21, 25 and 28 are unpatentable.

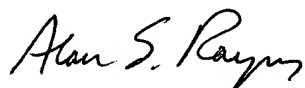
Applicant thanks the Examiner for indicating that claims 6 and 24 are allowed and that claims 15, 22, 26-27 and 33-35 would be allowable if rewritten to include all of limitations of the base claims and any intervening claims.

In the comments regarding allowable subject matter the Examiner provided various reasons for the allowable subject matter. Applicant notes that the claims are directed to various combinations of features. It is respectfully submitted that the patentability of each of the allowed and allowable claims resides in the combination of features recited in that claim in addition to any features noted by the Examiner.

The Office Action also included various comments concerning the art and the non-patentability of features in various of the pending claims. Applicants respectfully disagree with the Examiner's non-patentability conclusions. The discussion above has directly addressed some of those comments and the Examiner's other comments are deemed moot at this time in view of this response.

For at least the above reasons, applicant respectfully submits that claims 1-35 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,



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Dated: *July 7, 2003*

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 July 7, 2003
Alan S. Raynes (Date)